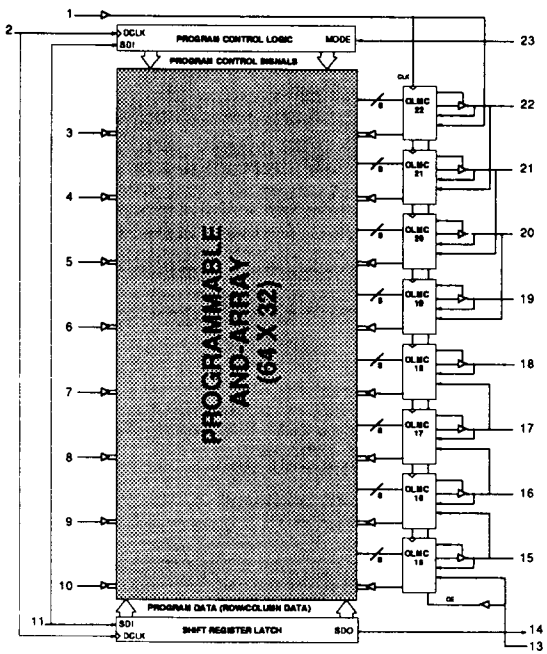
# ispGAL16Z8

**In-System Programmable**
**High Performance E²CMOS PLD**

## FEATURES

- **IN-SYSTEM-PROGRAMMABLE — 5-VOLT ONLY**
  - **— Change Logic "On The Fly" in Seconds**
  - **— Non-volatile E² Technology**
- **MINIMUM 10,000 ERASE/WRITE CYCLES**
- **DIAGNOSTIC MODE FOR CONTROLLING AND OBSERVING SYSTEM LOGIC**
- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 20 ns Maximum Propagation Delay**
  - **— Fmax = 41.6 MHz**
  - **— 90 mA MAX Icc**
- **E² CELL TECHNOLOGY**
  - **— 100% Tested/Guaranteed 100% Yields**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Reconfigurable Interfaces and Decoders**
  - **— "Soft" Hardware (Generic Systems)**
  - **— Copy Protection and Security Schemes**
  - **— Reconfiguring Systems for Testing**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

## FUNCTIONAL BLOCK DIAGRAM




## DESCRIPTION

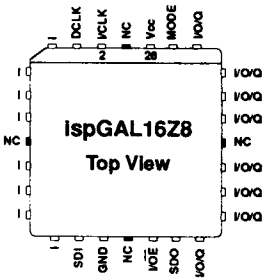
The Lattice ispGAL® 16Z8 is a revolutionary programmable logic device featuring 5-volt only in-system programmability and in-system diagnostic capabilities. This is made possible by on-chip circuitry which generates and shapes the necessary high voltage programming signals. Using Lattice's proprietary UltraMOS® technology, this device provides true bipolar performance at significantly reduced power levels.

The 24-pin ispGAL16Z8 is architecturally and parametrically identical to the 20-pin GAL16V8, but includes 4 extra pins to control in-system programming. These pins are not associated with normal logic functions and are used only during programming and diagnostic operations. This 4-pin interface allows an unlimited number of devices to be cascaded to form a serial programming and diagnostics loop.

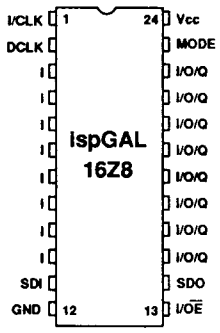
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. Therefore, LATTICE is able to guarantee 100% field programmability and functionality of all GAL® products.

## PIN CONFIGURATION

**PLCC**




**DIP**

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## ABSOLUTE MAXIMUM RATINGS[1]

Supply voltage $V_{CC}$ ..... -0.5 to +7V
Input voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Off-state output voltage applied ..... -2.5 to $V_{CC}$ +1.0V
Storage Temperature ..... -65 to 150°C
Ambient Temperature with
Power Applied ..... -55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

## RECOMMENDED OPERATING COND.

Ambient Temperature ($T_A$) ..... 0 to +75°C
Supply voltage ($V_{CC}$)
with Respect to Ground ..... +4.75 to +5.25V

## DC ELECTRICAL CHARACTERISTICS

**Over Recommended Operating Conditions (Unless Otherwise Specified)**

| SYMBOL | PARAMETER | CONDITION | MIN. | TYP.[2] | MAX. | UNITS |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | Vss – 0.5 | — | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | — | Vcc+1 | V |
| $I_{IL}$ | Input or I/O Low Leakage Current | $0V \le V_{IN} \le V_{IL}$ (MAX.) | — | — | –10 | µA |
| $I_{IH}$ | Input or I/O High Leakage Current | $V_{IH} \le V_{IN} \le V_{CC}$ | — | — | 10 | µA |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | — | — | 0.5 | V |
| $V_{OH}$ | Output High Voltage | $I_{OH}$ = MAX. Vin = $V_{IL}$ or $V_{IH}$ | 2.4 | — | — | V |
| $I_{OL}$ | Low Level Output Current | | — | — | 24 | mA |
| $I_{OH}$ | High Level Output Current | | — | — | –3.2 | mA |
| $I_{OS}$[1] | Output Short Circuit Current | $V_{CC}$ = 5V $V_{OUT}$ = 0.5V $T_A$ = 25°C | –30 | — | –150 | mA |
| $I_{CC}$ | Operating Power Supply Current | VIL = 0.5V VIH = 3.0V<br>ftoggle = 15Mhz Outputs Open | — | 75 | 90 | mA |

1) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems caused by tester ground degradation. Guaranteed but not 100% tested.
2) Typical values are at Vcc = 5V and $T_A$ = 25 °C

## CAPACITANCE ($T_A$ = 25 C, f = 1.0 MHz)

| SYMBOL | PARAMETER | MAXIMUM* | UNITS | TEST CONDITIONS |
|---|---|---|---|---|
| $C_I$ | Input Capacitance | 8 | pF | $V_{CC}$ = 5.0V, $V_I$ = 2.0V |
| $C_{I/O}$ | I/O Capacitance | 10 | pF | $V_{CC}$ = 5.0V, $V_{I/O}$ = 2.0V |

*Guaranteed but not 100% tested.

## AC SWITCHING CHARACTERISTICS

**Over Recommended Operating Conditions**

| PARAMETER | TEST COND.[1] | DESCRIPTION | -20 | | -25 | | UNITS |
|---|---|---|---|---|---|---|---|
| | | | MIN. | MAX. | MIN. | MAX. | |
| $t_{pd}$ | 1 | Input or I/O to Combinational Output | 3 | 20 | 3 | 25 | ns |
| $t_{co}$ | 1 | Clock to Output Delay | 2 | 15 | 2 | 15 | ns |
| $t_{su}$ | — | Setup Time, Input or Feedback before Clock↑ | 15 | — | 20 | — | ns |
| $t_h$ | — | Hold Time, Input or Feedback after Clock↑ | 0 | — | 0 | — | ns |
| $f_{max}$[2] | 1 | Maximum Clock Frequency with External Feedback, 1/(tsu + tco) | 33.3 | — | 28.5 | — | MHz |
| | 1 | Maximum Clock Frequency with No Feedback | 41.6 | — | 33.3 | — | MHz |
| $t_{wh}$[3] | — | Clock Pulse Duration, High | 12 | — | 15 | — | ns |
| $t_{wl}$[3] | — | Clock Pulse Duration, Low | 12 | — | 15 | — | ns |
| $t_{en}$ | 2 | Input or I/O to Output Enabled | — | 20 | — | 25 | ns |
| | 2 | OE↓ to Output Enabled | — | 18 | — | 20 | ns |
| $t_{dis}$ | 3 | Input or I/O to Output Disabled | — | 20 | — | 25 | ns |
| | 3 | OE↑ to Output Disabled | — | 18 | — | 20 | ns |

1) Refer to **Switching Test Conditions** section.
2) Refer to **fmax Description** section.
3) Clock pulses of widths less than the specification may be detected as valid clock signals.

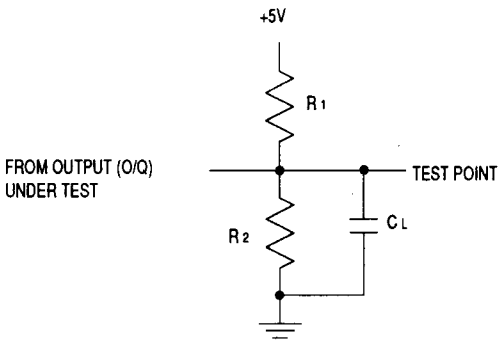
## SWITCHING TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns 10% – 90% |
| Input Timing Reference Levels | 1.5V |
| Output Timing Reference Levels | 1.5V |
| Output Load | See Figure |

3-state levels are measured 0.5V from steady-state active level.

**Output Load Conditions (see figure)**

| Test Condition | | $R_1$ | $R_2$ | $C_L$ |
|---|---|---|---|---|
| 1 | | 200Ω | 390Ω | 50pF |
| 2 | Active High | ∞ | 390Ω | 50pF |
| | Active Low | 200Ω | 390Ω | 50pF |
| 3 | Active High | ∞ | 390Ω | 5pF |
| | Active Low | 200Ω | 390Ω | 5pF |




C L INCLUDES JIG AND PROBE TOTAL CAPACITANCE

## ispGAL16Z8 ORDERING INFORMATION

### Commercial Grade Specifications

| Tpd (ns) | Tsu (ns) | Tco (ns) | Icc (mA) | Ordering # | Package |
|---|---|---|---|---|---|
| 20 | 15 | 15 | 90 | ispGAL16Z8-20LP | 24-Pin Plastic DIP |
| | | | 90 | ispGAL16Z8-20LJ | 28-Lead PLCC |
| 25 | 20 | 15 | 90 | ispGAL16Z8-25LP | 24-Pin Plastic DIP |
| | | | 90 | ispGAL16Z8-25LJ | 28-Lead PLCC |

## PART NUMBER DESCRIPTION